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RESUME OF GARY F. WITTING

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SUMMARY

Extensive experience in both intellectual property and technology. Developed management systems to provide intellectual property management, including patent prosecution, portfolio management, client counseling, and patent portfolio development and analysis. Strategic use of intellectual property to generate revenue and set the stage for business development of new technology.

KEY QUALIFICATIONS

- Strategic Use of Intellectual Property
- Intellectual Property Planning
- Contracts
- Licensing
- Negotiation
- Patent Prosecution
- Disclosure Review
- Patent Review

PROFESSIONAL EXPERIENCE

THE LAW FIRM OF GARY F. WITTING, Scottsdale, AZ

2004-

Patent Attorney/Intellectual Property Manager

Intellectual Property/Technology Law

- An intellectual/technology law firm dealing at the intersection of law, technology, science, business, and art.
- The firm helps the entrepreneur and seasoned professional to develop, protect, and exploit their intellectual property assets.

MOTOROLA, INC., Tempe, AZ

1979-2004

Patent Attorney/Intellectual Property Manager

1998-2004

Physical Science Research Laboratories (PSRL)

- Established processes and management tools to implement portfolio management that provided a means to review patterns that might result in future business development opportunities.
- Implemented management of the Intellectual property, including patents, copyrights, trademarks, trade secrets.
- Wrote and prosecuted Motorola's 2003 Semiconductor Product Sector's Patent of the Year which has secured and is currently being licensed for large revenue streams.
- Initiated strategic use of intellectual property to enhance present and future position in the market place by licensing out a patent portfolio involving Organic Light Emitting Devices (OLED).

- Strategic licensing-out, licensing-in, and acquisition of technology, thereby positioned intellectual property assets for present and future market places, as well as enabling licensee(s) to join in the market.
- Initiated and chaired organization's Patent Committee that decides patentability and focus of patent disclosures.
- Developed business relationships by negotiating and providing legal support services for Joint Development, Consortia, and other business development tools so as to better position Motorola in the marketplaces of the present and in the future.

Registered Patent Agent, Intellectual Property Department, Scottsdale, AZ 1995-1998

- Prosecuted patent applications which secured patent protection for Motorola's advanced and key technologies through the Patent and Trademark Office.
- Provided business development support to PSRL while attending law school.

Patent Engineer/Registered Patent Agent, Intellectual Property Department 1993-1995

- Obtained registration as a Patent Agent to practice before the United States Patent and Trademark Office (July 9, 1993).
- Wrote and prosecuted some of Motorola's most advanced and key technology patents through the PTO.
- Areas of patent application prosecution expertise include chemical processing, optics, semiconductor device, and mechanical.

Patent Engineer 1989-1993

- Developed the capability to use the Automatic Patent Search (APS) system for evaluation of several factors such as relative worth among Motorola's own patents, exposing possible infringers of Semiconductor Product Sector patents, and prior art searches using the same data base that the patent examiners use at the United States Patent and Trademark Office.
- Identified patentable inventions, identifying possible infringers, and developing defensive strategies.

Process Engineer, Very High Speed Integrated Circuit (VHSIC) Submicron Development Group 1984-1989

- Researched and developed production worthy deposition processes using an Applied Material 5000 Chemical Vapor Deposition system for fabricating integrated circuits.
- Researched and developed a production worth trench etches process for submicron bipolar VHSIC products.
- Researched and developed the first optical photolithographic process for submicron features.
- Researched and developed a selective tungsten deposition process for vias with depths ranging from 0.4u to 20.0u.

Principal Engineer, MOS5, Dram and MPU Manufacturing Facility, Mesa, AZ 1979-1984

- In charge of a three shift operation, engineering and production, of pre-nitride oxidation/Low Pressure Chemical Vapor Deposition (LPCVD) nitride sandwich structure while increasing capacity by over 90 percent and reducing particles by over 90 percent.
- Increased process yields of the previously mentioned sandwich structure from 69 percent to over 90 percent.
- Developed a wafer to wafer inspection system.
- Developed and provided a low phosphorus containing film suitable for dielectric layer in Very Large Scaled Integrated Circuit (VLSIC) fabrication.
- Developed a plasma metal etch process for patterning metal lines for VLSICs.

- Developed a sloped electrical contact for manufacturing VLSICs.

BARROW NEUROLOGIC INSTITUTE, Phoenix, AZ

1972-1977

Research Associate

- Designed and conducted independent experiments on immunological effects of morphine dependency.
- Designed and managed experimental programs involving basic mechanisms of suppressor cell function, as well as their relation to hypersensitivity.
- Conducted experiments relating to pharmacological behavioral psychology.

EDUCATION

Juris Doctorate, Franklin Pierce Law Center
Bachelor's of Science, Arizona State University
Associated of Arts, Scottsdale Community College

ASSOCIATIONS

Member of the Arizona State Bar Association
Member of the Arizona patent Law Association
Member of Licensing Executive Society
Member of the American Intellectual Property Lawyers Association

LICENSES

Licensed to practice law before the United States Patent and Trademark Office
Licensed to practice law before the Arizona State Court System
Licensed to practice law before the United States District Court for the District of Arizona

PUBLICATIONS/PRESENTATIONS

KODAK MICRO ELECTRONIC SYMPOSIUM 1987

A Manufacturable 0.5-micron optical lithography process.

Presented A Brief Tutorial on Intellectual Property to the Phoenix Area Consultants Network (PACN) chapter of the Institute of Electrical and Electronics Engineers (IEEE) .

Letter in response to: IS IP SAFE IN CHINA published in Electronic Business
<http://www.reed-electronics.com/eb-mag/article/CA386092?industryid=2119>

ISSUED PATENTS

Title	Patent Number
Self-aligned Transistor Method	4,728,606
Selective Metal Deposition Process	4,853,347
Optical Reading Head with Angled Array	5,349,210
Optical Reading Head with Angled Array	5,466,633
Method for Making Optical Interface Unit with Detachable Photonic Device	5,522,002
Electronic Book	5,534,888
Optical Interface Unit with Detachable Photonic Device	5,625,732
Integrated Light Emitting Device	5,546,413

PATENTS WRITTEN

	Patent Number	Title
1	5,164,093	Apparatus and method for removing Metallic contamination from fluids using silic on beads
2	5,149,674	Method for making a planar Multi-layer metal bonding pad
3	5,170,448	Optical waveguide apparatus and method for partially collecting light
4	5,273,850	Chromeless phase-shift mask and method for making
5	5,229,305	Method for making intrinsic gettering sites in bonded substrates
6	5,138,237	A field emission electron device employing a modulatable diamond semiconductor emitter
7	5,313,545	Molded waveguide with unitary cladding region and method of making
8	5,369,529	Reflective optoelectronic interface device and method of making
9	5,265,184	Molded waveguide and method for making same
10	5,164,328	Method of bump bonding and sealing an accelerometer chip onto an integrated circuit chip
11	5,068,007	Etching of materials in a noncorrosive environment
12	5,045,908	Vertical and laterally illuminated P-I-N photodiode
13	5,080,933	Selective deposition of polycrystalline silicon
14	5,131,968	Gradient chuck method for wafer bonding employing a convex pressure
15	5,034,092	Plasma etching of semiconductor substrates
16	5,209,117	Tapered cantilever beam for sensors

17	5,233,861	Apparatus and method for in situ calibration of metering device
18	5,187,347	Susceptor electrode and method for making same
19	5,146,416	Method and apparatus for accurately measuring thickness of a semiconductor die bonding material
20	5,116,460	Method for selectively etching a feature
21	5,230,184	Distributed polishing head
22	5,116,461	Method for fabricating an angled diffraction grating
23	5,256,888	Transistor device apparatus employing free -space electron emission from a diamond material surface
24	5,249,245	Optoelectronic mount including flexible substrate and method for making same
25	5,276,754	Optoelectronic mount and method for making
26	5,337,397	Optical coupling device and method for making
27	5,242,103	Pivotal wire bonding stage and method of use
28	5,309,537	Optoelectronic coupling device and method of making
29	5,325,451	Modular optical waveguide and method for making
30	5,317,587	VCSEL with separate control of current distribution and optical mode
31	5,337,391	Optoelectronic sub-module and method of making same
32	5,319,192	Wavelength discriminable optical signal detector insensitive to variation in optic signal intensity
33	5,661,075	Method of making a VCSEL with passivation
34	5,650,356	Method for reducing corrosion in openings on a semiconductor wafer
35	5,636,298	Coalescing optical module and method for making
36	5,625,732	Optical interface unit with detachable photonic device
37	5,604,640	Business card scanner and method of use
38	5,590,239	Planar uniform heating surface with additional circumscribing ring
39	5,578,906	Field emission device with transient current source
40	5,574,744	Optical coupler
41	5,555,341	Waveguide with an electrically conductive channel
42	5,552,247	Method for patterning an X-ray master mask
43	5,550,941	Optoelectronic interface module
44	5,547,898	Method for p-doping of a light-emitting device
45	5,546,413	Integrated light emitting device
46	5,545,359	Method of making a plastic molded optoelectronic interface
47	5,539,200	Integrated optoelectronic substrate
48	5,534,888	Electronic book
49	5,530,715	Vertical cavity surface emitting laser having continuous grading
50	5,522,002	Method for making optical interface unit with detachable photonic device
51	5,521,992	Molded optical interconnect
52	5,517,348	Voltage controlled transparent layer for a bi -directional device
53	5,511,138	Interlocking waveguide and method of making
54	5,500,914	Optical interconnect unit and method or making
55	5,482,891	VCSEL with an integrated heat sink and method of making
56	5,482,658	Method of making an optoelectronic interface module
57	5,468,656	Method of making a VCSEL
58	5,468,582	Fused optical layer and method of making
59	5,466,633	Optical reading head and method for making same
60	5,453,401	Method for reducing corrosion of a metal surface containing at least aluminum and copper
61	5,452,387	Coaxial optoelectronic mount and method of making same

62	5,449,435	Field emission device and method of making the same
63	5,446,814	Molded reflective optical waveguide
64	5,444,289	Vertical and lateral isolation for a semiconductor device
65	5,439,753	Electron emissive film
66	5,437,092	Method of making contact areas on an optical waveguide
67	5,430,348	Inversion mode diamond electron source
68	5,428,704	Optoelectronic interface and method of making
69	5,416,870	Optoelectronic interface device and method with reflective surface
70	5,400,423	Molded star coupler and method of making same
71	5,390,275	Molded waveguide and method for making same
72	5,389,569	Vertical and lateral isolation for a semiconductor device
73	5,384,873	Optical interface unit and method of making
74	5,369,529	Reflective optoelectronic interface device and method of making
75	5,349,210	Optical reading head with angled array
76	5,345,530	Molded waveguide and method for making same
77	5,345,524	Optoelectronic transceiver sub-module and method for making
78	5,337,397	Optical coupling device and method for making
79	5,337,391	Optoelectronic sub-module and method of making same
80	5,325,451	Modular optical waveguide and method for making
81	5,319,192	Wavelength discriminable optical signal detector insensitive to variations in optical signal intensity
82	5,313,545	Molded waveguide with a unitary cladding region and method of making
83	5,313,140	Field emission device with integral charge storage element and method for operation
84	5,309,537	Optoelectronic coupling device and method of making
85	5,287,002	Planar multi-layer metal bonding pad
86	5,286,581	Phase-shift mask and method for making
87	5,282,071	Contact areas on an optical waveguide and method of making
88	5,276,754	Optoelectronic mount and method for making
89	5,273,850	Chromeless phase-shift mask and method for making
90	5,249,245	Optoelectronic mount including flexible substrate and method for making same
91	5,242,103	Pivotal wire bonding stage and method of use

* Some of these patents were ghost written and other patents have been omitted.